REMARKS

Objection to the Drawings

Fig. 2 was objected to because it includes the reference character "218" that was not mentioned in the description. In response thereto, Fig. 2 has been amended by removing "218" and the corresponding lead line from between the test head 205 and the DUT 116 in Fig. 2.

In addition, a minor informality was identified in Fig. 3, which has also been amended. The size of blocks 308 and 310, located in the middle of the drawing, has been increased in order that the entire term "Combinational" can be shown all on one line.

Response To Objections To Specification

The specification has been objected to because the term "test sequence" is defined as "a series of test vectors" in one portion of the specification and defined as "containing a plurality of bits" in another. The Office Action suggests that these statements are contradictory. In response thereto, Applicants respectfully traverse this objection and assert that these statements do not contradict each other.

Applicants direct the Examiner's attention to p. 3, lines 4-12 of the present specification. In this passage of the specification, the terms "test vector" and "test sequence," *inter alia*, are defined. A test vector is defined as a string of n logic values (0, 1, or don't care - X). These logic values, of course, are bit values. A test sequence is defined as a series of test vectors. It logically follows that since a test vector is a string of logic values or bits, and a test sequence is a series of test vectors, then the test sequence is a series of strings of logic values or bits. Thus, a test sequence, as defined, contains a plurality of bits.

In light of the definitions presented on p. 3, lines 4-12, Applicants contend that the specification adequately defines the terms in such a way that one of ordinary skill would be able to clearly understand the invention and that one of ordinary skill would be led by the specification to the conclusion that a test sequence contains a plurality of bits. Therefore, Applicants respectfully request that the Examiner kindly withdraw the objection to the specification.

Response To Objection To Abstract

The abstract is objected to because it cites "each test sequence of the set of test sequences containing a plurality of bits," which allegedly contradicts the definition provided on p. 3, lines 6-7. As mentioned above, Applicants contend that the definition of the specification sufficiently provides support for the concept of the test sequence including a plurality of bits, based on the logic that a test sequence is defined as being a series of test vectors, and the test vectors are defined as being a string of bits. For this reason, the abstract does not contradict the specification. Applicants therefore request that the objection to the abstract be withdrawn.

Response To Claim Rejections Under 35 U.S.C. §112, First Paragraph

Claims 1-20 stand rejected under 35 U.S.C. §112, first paragraph, as not being enabling to one skilled in the art. The Office Action states that the phrase "each test sequence of the set of test sequences containing a plurality of bits" (in the claims) contradicts the definition provided on p. 3, lines 6-7. As mentioned above, Applicants assert that no contradiction exists and that p. 3, lines 4-12 adequately define the test sequence as inherently containing a plurality of bits. Therefore, the claims are believed to be free of contradiction and clear to one skilled in the art. Applicants respectfully request that the rejection of claims 1-20 be withdrawn in light of the definition of terms presented in p. 3, lines 4-12.

Response To Claim Rejections Under 35 U.S.C. §112, Second Paragraph

Claims 1-20 stand rejected under 35 U.S.C. §112, second paragraph, as being incomplete for omitting essential structurally cooperative relationships of elements, namely the relationship between "test sequence" and a "plurality of bits." As mentioned above, p. 3, lines 4-12 of the specification define a "test vector" as a string of logic bits having values of 0, 1, or X (don't care; 0 or 1) and a "test sequence" as a series of test vectors. Hence, a test sequence contains a plurality of bits. Applicants request that the rejection of claims under 35 U.S.C. §112, second paragraph be withdrawn.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and rejections have been traversed, and that the pending claims 1-20 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned agent at (770) 933-9500.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, Washington D.C. 20231, on March 11, 2003.

Evelyn Sanders
Signature – Evelyn Sanders